This mode begins when Q2 is turned off at t0. At this moment, resonant inductor Lr current is negative; it will flow through body diode of Q1, which creates a ZVS condition for Q1. Gate signal of Q1 should be applied during this mode.

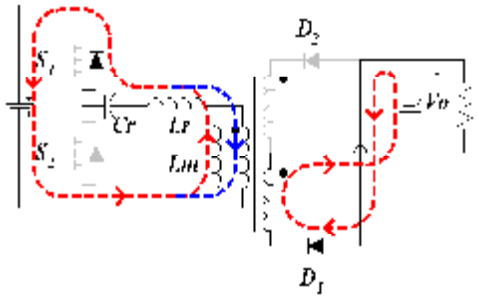


Figure 4.18 Circuit diagram during mode 1 in region 2

When resonant inductor Lr current flow through body diode of Q1, I_{Lr} begins to rise, this will force secondary diode D1 conduct and Io begin to increase. Also, from this moment, transformer sees output voltage on the secondary side. Lm is charged with constant voltage.

Mode 2 (t1 to t2)

This mode begins when resonant inductor current I_{Lr} becomes positive. Since Q1 is turned on during mode 1, current will flow through MOSFET Q1.

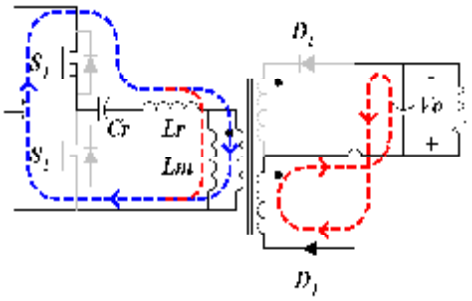


Figure 4.19 Circuit diagram during mode 2 in region 2

During this mode, output rectifier diode D1 conduct. The transformer voltage is clamped at Vo. Lm is linearly charged with output voltage, so it doesn't participate in the resonant during this period. In this mode, the circuit works like a SRC with resonant inductor Lr and resonant capacitor Cr.

This mode ends when Lr current is the same as Lm current. Output current reach zero.

Mode 3 (t2 to t3)

At t2, the two inductor's currents are equal. Output current reach zero. Both output rectifier diodes D1 and D2 is reverse biased. Transformer secondary voltage is lower than output voltage. Output is separated from transformer.

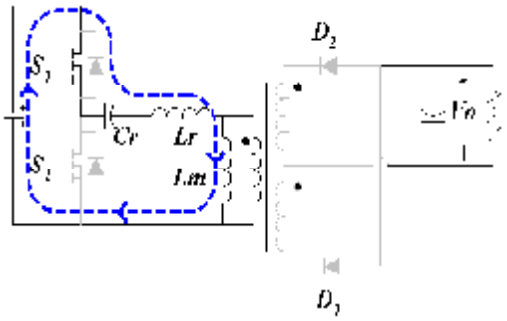


Figure 4.20 Circuit diagram during mode 3 in region 2

During this period, since output is separated from primary, Lm is freed to participate resonant. It will form a resonant tank of Lm in series with Lr resonant with Cr.

This mode ends when Q1 is turned off. As can be seen from the waveform, Q1 turn off current at t3 is small compare with peak current. For next half cycle, the operation is same as analyzed above.

From the simulation waveform we can see, the MOSFETs are turned on with ZVS. The ZVS is achieved with magnetizing current, which is not related to load current, so ZVS could be realized even with zero-load. Since this magnetizing current is also the turn off current of MOSFET. Choosing different magnetizing inductance could control it. The turn off current could be much smaller than load current, so turn off loss can be reduce. Also, the secondary side diode current reduce to zero and stay off, the reverse recovery is eliminated also. With all these, the switching loss of this converter is very small.

4.5 Design of LLC resonant converter

4.5.1 Design of power stage parameters

From above analysis, the DC characteristic of LLC resonant converter could be derived. Based on the DC characteristic, parameters in power stage can be designed. The parameters need to be designed are:

- Transformer turns ratio: n
- Series resonant inductor: Lr
- Resonant capacitor: Cr
- Resonant inductor ratio: Lm/Lr

The specifications for the design are:

Input voltage range: 300V to 400V, normal operating region (360-400V)

Output voltage: 48V

Maximum load: 2.5Ohm

Maximum switching frequency: 200kHz

With above information, we can begin to choose the parameters.

For front-end application, the target is to optimize the performance at high input voltage. From previous analysis results, the optimal operating point for this

converter is when switching frequency equals to the resonant frequency of Lr and Cr. At this point, the voltage gain of LLC resonant converter is 1. Base on this, the transformer turns ratio can be choose. For Half Bridge LLC resonant converter with 400V input and 48V output, the transformer turns ratio can be choose base on following equations:

$$n = Vin/(2 \cdot Vo)$$

For Full Bridge LLC resonant converter, the turn's ratio will be:

$$n - Vin/Vo$$

In our design, a half bridge LLC resonant converter is used; the turns ratio was choose to be 4.

After the transformer turns ratio, the resonant tank can be designed. To determine the resonant tank, lot of trade offs are involved. Three design examples will be shown to demonstrate the trade offs.

Design 1:

In this design, the ratio of two resonant inductors is 1, which means the two resonant inductors are with same value. The characteristic and operating region are shown in Figure 4.21. The region of Q is from 1(Full load) to 0(no load). Here Q is defined as: Q=Zo/Rl. Resonant inductor Lr is 27.8uH, resonant inductor Lm is 27.8uH and Cr is 22.8nF.

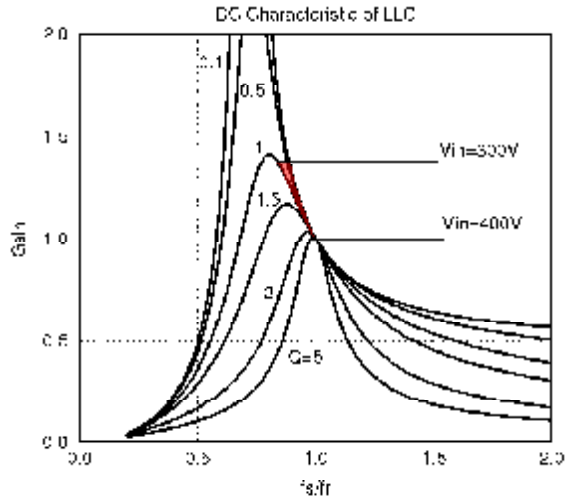


Figure 4.21 Operating region for design 1

Simulation waveform is shown in Figure 4.22.

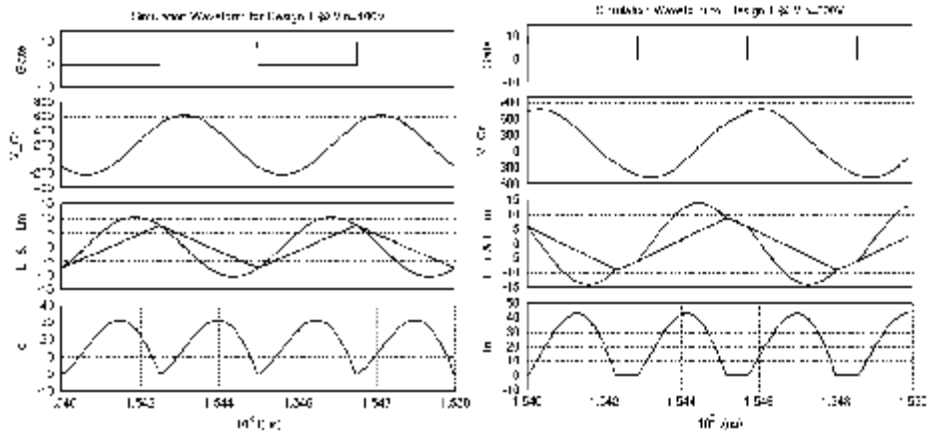


Figure 4.22 Simulation waveforms of design 1 with 300V and 400V input voltage

Design 2:

In this design, the ratio of two resonant inductors is 4, which means Lm is four times Lr. The characteristic and operating region are shown in Figure 4.23.

The region of Q is from 0.5 (Full load) to 0 (no load). Resonant inductor Lr is 17uH and Lm is 70uH. Resonant capacitor is 24nF.

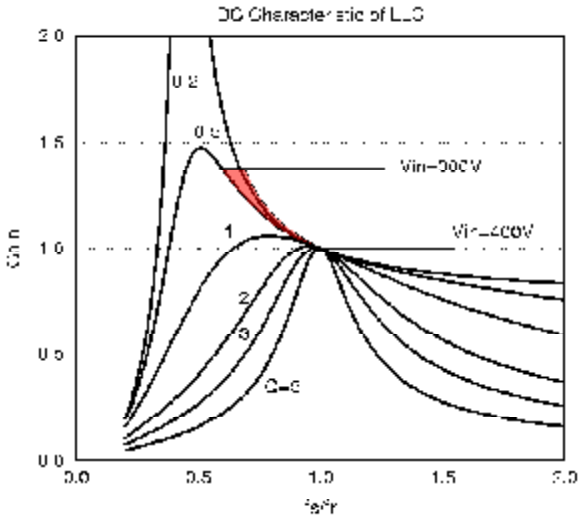


Figure 4.23 Operating region for design 2

Simulation waveform is shown in Figure 4.24.

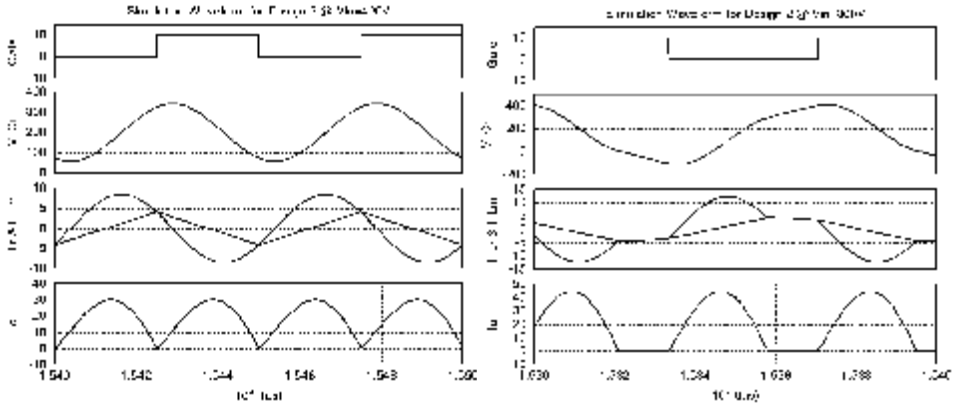


Figure 4.24 Simulation waveforms of design 2 with 300V and 400V input voltage

Design 3:

In this design, the ratio of two resonant inductors is 16, which means Lm is sixteen times Lr. The characteristic and operating region are shown in Figure 4.25. The region of Q is from 0.25 (Full load) to 0 (no load). Resonant inductor Lr is 7.95uH, Lm is 127uH and Cr is 79.6nF.

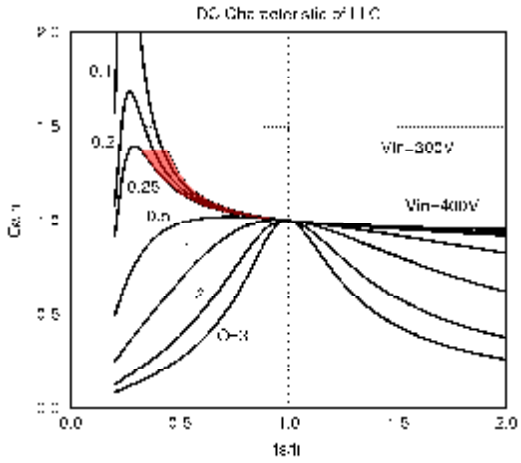


Figure 4.25 Operating region for design 3

Simulation waveform is shown in Figure 4.26.

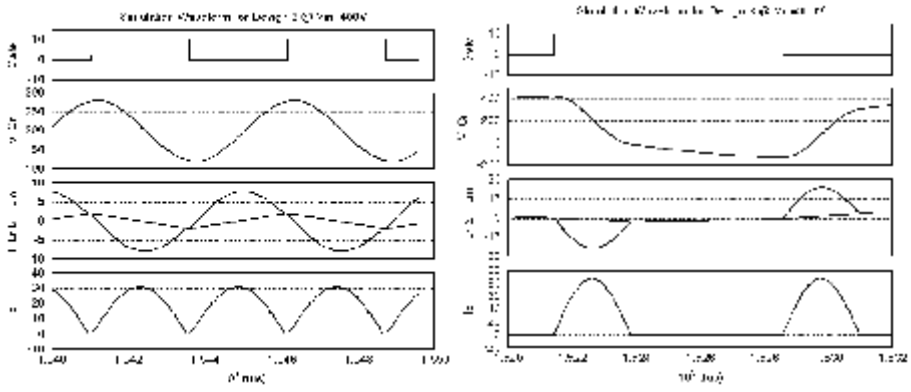


Figure 4.26 Simulation waveforms of design 3 with 300V and 400V input voltage

Summary of three designs:

Table 4-1 Summary of three LLC resonant converter designs

	Q range	*Fs range*	*Primary RMS Current*	*Switch turn off current*	*Resonant Cap Voltage*	*Peak Output current*
Design 1	1 to 0	175k to 200k	8.1A to 9.2A	7.8A to 5.8A	800V	31A to 43A
Design 2	0.5 to 0	135k to 200k	6.0A to 8.3A	4.1A to 3.2A	440V	31A to 49A
Design 3	0.25 to 0	72k to 200k	5.7A to 10.2A	1.9A to 0.24A	430V	31A to 89A

From the summary, design 3 provides best performance at 400V input, but the switching frequency range will be much larger. For design 1, the performance at 400V is compromised; the benefit is very narrow switching frequency range. For this application, since the output voltage of PFC circuit is not tightly regulated, it has a range from 360 to 400V. The performance at 360V is also a concern. In Figure 4.27 to Figure 4.29, primary switching and conduction loss are compared for three designs with different input voltage.

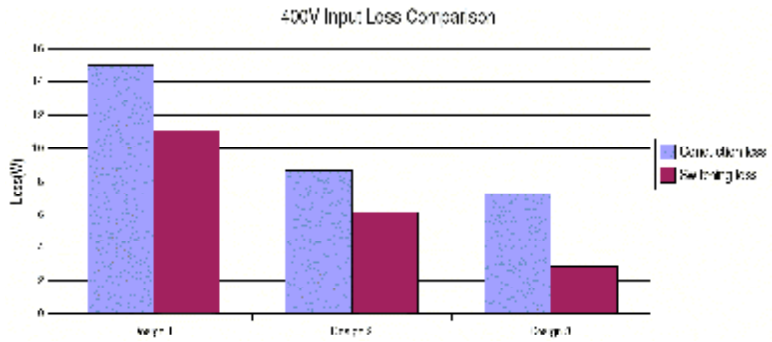


Figure 4.27 Primary loss for three designs with Vin=400V

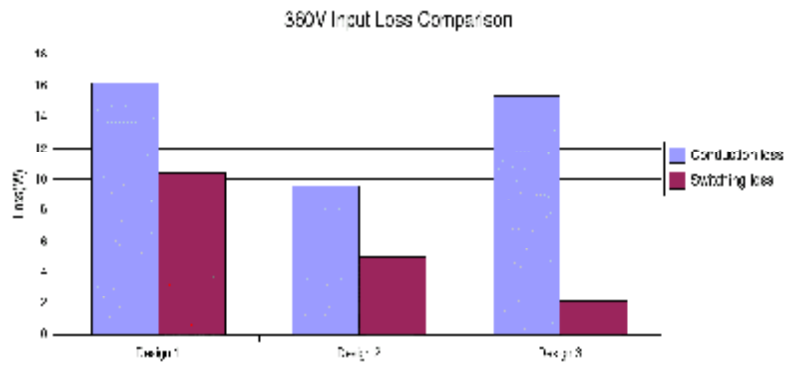


Figure 4.28 Primary loss for three designs with Vin=360V

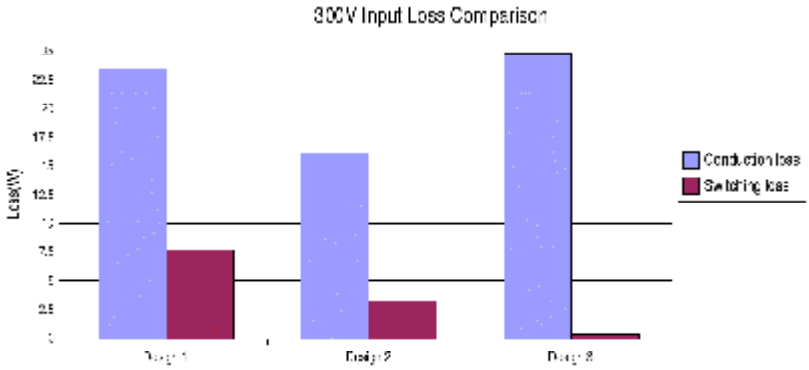


Figure 4.29 Primary loss for three designs with Vin=300V

From these comparisons, although design 3 could provide better performance at 400V input, its performance degrades very fast as input voltage drops. Design 1 could provide more balanced performance for whole range, but the performance at 400V input is greatly impaired. Design 2 is choosing for front-end application with 200kHz design. With design 2, the performance is balanced within input range. Stress on different devices is reasonable.

4.5.2 Design trade offs:

In design of power stage, there are some trade offs that will affect the final results.

First trade off is switching frequency range and switching loss. With smaller magnetizing inductance, narrower switching frequency range can be achieved, but switching loss and conduction loss will increase because of high magnetizing current.

Another trade off to make is switching frequency range and resonant tank impedance. For same specification, Lr and Cr can have different values, which will work. Although there is a limit on how small Cr can be in order to keep series resonant tank work in constant gain region. With larger Cr, the voltage stress on Cr will be smaller. The problem is that the impedance of the resonant tank will be small too, which will affect the short circuit performance. With smaller tank impedance, the higher the shorts circuit current will be and higher switching frequency is needed to limit the output current.

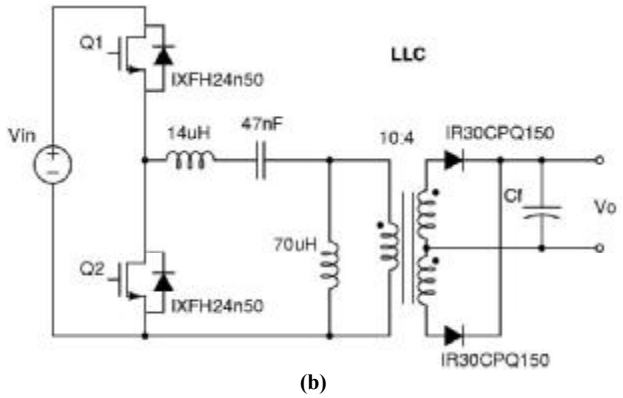
The problem with low switching frequency is the conduction loss will increase as switching frequency drops. As shown in first part, the conduction loss can be doubled when switching frequency change from 200kHz to 150kHz.

From these trade offs, the optimized design should choose as small resonant capacitor as possible to get enough voltage gain at heavy load. Then Lm should

be as large as possible to get the voltage gain with desired switching frequency range.

4.5.3 Test results

Base on the design, a LLC resonant converter is built with those parameters. The test circuits are shown in Figure 4.30 with the part number of the devices. Test waveforms are shown in Figure 4.31. The test efficiency is shown in Figure 4.32. Compare with asymmetrical half bridge converter, LLC resonant converter could improve the efficiency at normal operation point by more than 3%. Figure 4.33 shows the test efficiency at different input voltage. LLC resonant converter could cover wide input range with much higher efficiency compared with PWM converter.



(b)

Figure 4.30 Test circuit for 200kHz LLC resonant converter